PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Mark R. Sikkink et al. Examiner: Daniel Ryman

Serial No.: 09/621,315 Group Art Unit: 2665

Filed: July 20, 2000 Docket: 499.081US1

For: AN INTERFACE FOR SYNCHRONOUS DATA TRANSFER BETWEEN DOMAINS CLOCKED AT DIFFERENT FREQUENCIES

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on August 29, 2005, from the Final Rejection of claims 1, 3-6, 8-10, 14-16, and 18 of the above-identified application, as set forth in the Final Office Action mailed on March 28, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, SILICON GRAPHICS, INC.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on July 20, 2000, with claims 1-19. A non-final Office action was mailed May 4, 2004. A response filed November 4, 2004 canceled claims 2, 7, 11-13, 17 and 19 and amended claims 1, 3, 5, 6, 10, 14 and 15. A Final Office Action (hereinafter "the Final Office Action") was mailed March 28, 2005. Claims 1, 3-6, 8-10, 14-16 and 18 stand rejected and are the basis for this appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated March 28, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

In modern microprocessor design, it is possible for the processor to be clocked at one frequency while the memory is clocked at a frequency that that is a less than that frequency. For example, it is possible to clock the processor at 200 MHz, while clocking the memory at 100, 114, 133 or 160 MHz (frequency ratios of 2:1, 7:4, 3:2, 5:4, respectively). What was recognized by Appellant is that, with the proper design, it is possible to provide a single design that provides synchronous data transfer across two or more frequency ratios. P. 9, lines 7-13.

To accomplish this, Appellant illustrates at Figs. 5-7, describes at p. 5, line 9 through p. 8, line 5, and claims in claims 1, 3-5, 15, 16 and 18, an interface for synchronous data transfer from a first domain (e.g., the processor domain) clocked at by a first clock at a first frequency to a second domain (e.g., the memory domain) clocked by a second clock at a slower frequency. The interface includes a first latch for receiving data from the first domain when the first latch is selected, a second latch for receiving data from the first domain when the second latch is selected, and a third latch for transferring data from said first latch or said second latch to the second domain when the second domain is clocked by a clock pulse of the second clock. The third latch is selectively toggled to receive data from the first latch or the second latch in response to a negative edge of the clock pulse clocking the second domain.

The first and second latches are clocked by the first clock at the first clock frequency and the first clock clocking the first domain and the second clock clocking the second domain are both derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated as a function of the same primary clock.

Appellant also illustrates at Figs. 8 and 9, describes at p. 8, line 6 through p. 9, line 1, and claims in claims 6, 8-10 and 14, an interface for synchronous data transfer between a first domain clocked at one frequency (e.g., the memory domain) and a second domain clocked at a faster frequency (e.g., the processor domain). The interface includes a first latch for receiving data from the first domain when the first latch is selected, a

second latch for receiving data from the first domain when the second latch is selected, and a third latch selectively toggled to receive data from said first latch or said second latch in response to a negative edge of a clock pulse, other than a hold pulse, clocking the second domain. The third latch transfers data from the first latch or the second latch to the second domain when the second domain is clocked by a next clock pulse that is not a hold clock pulse.

The first clock clocking the first domain and the second clock clocking the second domain are both derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated as a function of the same primary clock.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellants refer to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Were claims 1, 3-6, 8-10, 14-16, and 18 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Huon et al. (U.S. Patent No. 5,761,735) in view of Duffy (U.S. Patent No. 6,535,527) in further view of Santahuhta (EP 0989484) and in further view of Khandekar et al. (U.S. Patent No. 6,049,887)?

7. ARGUMENT

Rejections under U.S.C. § 103

1) The Applicable Law

According to *M.P.E.P.* § 2141, which cites *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986), the following tenets of patent law must be adhered to when applying 35 U.S.C. § 103. First, the claimed invention must be considered as a whole. Second, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination. Third, the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention. Fourth, obviousness is determined using a reasonable expectation of success standard. Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. *M.P.E.P.* § 2141 (citing *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966)).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellants' disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). The references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the

references. *M.P.E.P.* § 2142 (citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)). In considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw there from. *M.P.E.P.* § 2144.01 (citing *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968)). However, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

In order to take into account the inferences which one skilled in the art would reasonably make, the examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time the invention was made. *M.P.E.P.* § 2141.03 (citing *Environmental Designs, Ltd. v. Union Oil Co*, 713 F.2d 693, 218 USPQ 865 (Fed. Cir. 1983), *cert. denied*, 464 U.S. 1043 (1984)).

> The examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. Knowledge of Appellants' disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. The tendency to resort to "hindsight" based upon Appellants' disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

M.P.E.P. § 2141.03.

2) Application of §103 to the Rejected Claims

Claims 1, 3-6, 8-10, 14-16, and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Huon et al. (U.S. Patent No. 5,761,735) in view of Duffy (U.S. Patent

No. 6,535,527) in further view of Santahuhta (EP 0989484) and in further view of Khandekar et al. (U.S. Patent No. 6,049,887).

Both Appellant and Huon describe circuits for synchronizing data transfers between a first and a second device operating at different data rates. In contrast to Huon, however, Appellant describes, and claims in claims 1, 3-6, 8-10, 14-16, and 18, a system for performing this transfer synchronously. As can be seen in Huon at Figs. 1 and 2 , and as is described at col. 3, the memory device of Huon generates strobe signals. The strobe signals load appropriate registers and the registers are then read into a processor using the processor clock.

As noted by the Examiner, Khandekar, like Appellant, describes a circuit for synchronizing data transfers between a first and a second device operating at different data rates when the clocks are both derived from a primary clock and repeat in a ratioed, systematic pattern.

As noted above, the Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that obviousness "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination" and that teachings of references can be combined *only* if there is some suggestion or incentive to do so. *Id.*

Here, the Examiner stated (in the final Office Action, at p. 5, lines 10-17) that it would have been obvious to combine Huon in view of Duffy in further view of Satahuata with Khandakar since Khandekar teaches that a synchronous transfer mechanism reduces transfer latency penalty over that of an asynchronous mechanism. As noted above Huon describes such an asynchronous mechanism.

As noted above, the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the

artisan would have found the claimed invention to have been obvious in light of the teachings of the references. *M.P.E.P.* § 2142 (citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)).

The Examiner's logic here is circular. He is stating that the combination of Huon, etc with Khandakar is taught or suggested by a statement in Khandakar that his approach is better than the asynchronous approach taught by those espousing an asynchronous approach (such as Huon). There is no analysis of what would have to be done to either circuit to arrive at the circuit described and claimed by Appellant.

The motivation suggested by the Examiner for such a combination is "in order to check for skew between the two clock signals." Appellant respectfully submits that such a teaching would motivate one skilled in the art to replace the teaching of Huon with that of Khandakar, not to combine the references.

Khandekar, like Appellant, does describe a circuit for synchronizing data transfers between a first and a second device operating at different data rates when the clocks are both derived from a primary clock and repeat in a ratioed, systematic pattern. Khandekar, however, solves the problem of transferring data between the two domains differently than does Appellant. For instance, Khandekar does not use a sync pulse to frame the ratioed, systematic pattern in a circuit which transfers data from a first domain to a second domain clocked by a slower frequency as required by claims 1, 2-5, 15, 16 and 18. (The mask signal the Examiner points to is used when going from a slower domain to a faster domain.)

In addition, there is no teaching or suggestion in Khandekar or in any of the other cited references to apply the approach described by Khandekar to the circuit described by Huon. Even if one did, the combined circuit would not look like the circuit shown in Figs. 5-8, described by Appellant and claimed in claims 1, 3-6, 8-10 and 14-16 and 18.

Finally, none of the cited references describe the use of a hold signal in conjunction with the secondary synch pulse as described by Appellant and claimed in claims 6, 8-10 and 14 or the use of the no-op state as described by Appellant and claimed in claims 15, 16 and 18.

8. SUMMARY

For the reasons argued above, claims 1, 3-6, 8-10, 14-16, and 18 were wrongly rejected under 35 U.S.C. 103(a) as being unpatentable over Huon et al. (U.S. Patent No. 5,761,735) in view of Duffy (U.S. Patent No. 6,535,527) in further view of Santahuhta (EP 0989484) and in further view of Khandekar et al. (U.S. Patent No. 6,049,887).

It is respectfully submitted that the art cited does not render the claim anticipated and that the claims are patentable over the cited art. Reversal of the rejection and allowance of the pending claim are respectfully requested.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28 day of February, 2006.

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Name Signature

CLAIMS APPENDIX

1. (Rejected) An interface for synchronous data transfer from a first domain clocked at by a first clock at a first frequency to a second domain clocked by a second clock at a slower frequency, comprising:

a first latch for receiving data from the first domain when the first latch is selected;

a second latch for receiving data from the first domain when the second latch is selected; and

a third latch for transferring data from said first latch or said second latch to the second domain when the second domain is clocked by a clock pulse of the second clock, said third latch being selectively toggled to receive data from said first latch or said second latch in response to a negative edge of the clock pulse clocking the second domain;

wherein the first and second latches are clocked by the first clock at the first clock frequency; and

wherein the first clock clocking the first domain and the second clock clocking the second domain are both derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated as a function of the same primary clock.

2. (Cancelled)

3. (Rejected) The interface of claim 1, wherein at least one clock pulse of the first domain clock is a non-operate (NOP) clock pulse in each repeated systematic pattern when no data from the first domain is loaded into either said first latch or said second latch to cause equal average data transfer between the first domain and the second domain.

4. (Rejected) The interface of claim 3, wherein the NOP clock pulse is selected to minimize latency and prevent the slower clocked domain from being overrun by the faster clocked domain.

5. (Rejected) The interface of claim 1, wherein said first and second latches are selected by a select signal, said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data.

6. (Rejected) An interface for synchronous data transfer between a first domain clocked at one frequency and a second domain clocked at a faster frequency, comprising:

a first latch for receiving data from the first domain when the first latch is selected;

a second latch for receiving data from the first domain when the second latch is selected; and

a third latch selectively toggled to receive data from said first latch or said second latch in response to a negative edge of a clock pulse, other than a hold pulse, clocking the second domain and said third latch transferring data from said first latch or said second latch to the second domain when the second domain is clocked by a next clock pulse that is not a hold clock pulse;

wherein a first clock clocking the first domain and a second clock clocking the second domain are both derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated as a function of the same primary clock.

7. (Cancelled)

8. (Rejected) The interface of claim 6, wherein the hold clock pulse is selected to minimize latency.

9. (Rejected) The interface of claim 6, wherein said first and second latches are alternately selected by a select signal, said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data.

10. (Rejected) An interface for synchronous data transfer between domains clocked at different frequencies, comprising:

a first latch for receiving data from a first domain clocked at one frequency when said first latch is selected;

a second latch for receiving data from the first domain when said second latch is selected; and

a third latch for transferring data from either said first latch or said second latch to a second domain clocked at another frequency;

wherein the first domain is clocked at a slower frequency than the second domain and wherein said third latch is loaded when the second domain is clocked by a clock pulse that is not a non-operate pulse.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Rejected) The interface of claim 10, wherein said third latch is alternately toggled to transfer data from said first or said second latch in response to a negative edge of a clock pulse clocking the second domain unless the clock pulse is a non-operate clock pulse.

15. (Rejected) A method for synchronous data transfer between clocked domains, comprising:

loading a first master latch with data from the first domain in response to a first domain clock pulse;

transferring the data loaded in the first master latch to the second domain through a slave latch in response to a second domain clock pulse;

toggling the slave latch to switch to receive data from a second master latch in response to a negative edge of the second domain clock pulse that is not a non-operate clock pulse;

loading the second master latch with data from the first domain in response to another first domain clock pulse;

transferring the data loaded in the second master latch to the second domain through the slave latch in response to another second domain clock pulse;

toggling the slave latch to switch to receive data from the first master latch in response to the negative edge of the clock pulse of the second domain clock that is not a non-operate clock pulse;

repeating a cycle of alternately loading the first and second master latches and transferring data to the second domain through the slave latch until a master clear signal is received by the slave and master latches; and

entering a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock;

wherein the clock pulses of the first domain and the second domain are both derived from a primary clock and repeat in a ratioed, systematic pattern framed by a secondary synch pulse.

16. (Rejected) The method of claim 15, further comprising: generating a signal in response to loading one of the first or second master latches to cause data to be loaded alternately into the first and second master latches.

17. (Cancelled)

18. (Rejected) The method of claim 15, wherein the non-operate state is selected to minimize latency in transferring the data between the domains.

19. (Cancelled)

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.